

10/645330

Sheet 2 of 3

PTO-1449 REPRODUCED INFORMATION DISCLOSURE CITATION IN AN APPLICATION		ATTORNEY DOCKET NO. 2037.1004-007	CONT. OF APPLICATION NO. 10/348,062
August 21, 2003 (Use several sheets if necessary)		APPLICANT Richard C. Foss, et al.	
		FILING DATE	CONFIRMATION NO.
			GROUP

FOREIGN PATENT DOCUMENTS					
		DOCUMENT NUMBER	DATE	COUNTRY	TRANSLATION YES NO
MR	AL	JP-0214094	08/1990	Japan	XBS
	AM				
	AN				
	AO				
	AP				
	AQ				
	AL2				
	AM2				
	AN2				
	AO2				
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EXAMINER M. TRAN	DATE CONSIDERED 4/1/04
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		APPLICANT Richard C. Foss, et al.		
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U.S. PATENT DOCUMENTS				
EXAMINER INITIAL	REF. NO.	DOCUMENT NUMBER	ISSUE DATE / PUBLICATION DATE	NAME
PL	AA	4,754,164 307	June 28, 1988	Flora et al.
	AB	5,287,319 365	Feb. 15, 1994	Fukumoto
	AC	5,311,483 365	May 10, 1994	Takasugi
	AD	5,544,203 375	Aug. 6, 1996	Casasanta et al.
WV	AE	5,604,775 375	Feb. 18, 1997	Saitoh et al.
	AF	5,754,164 327	June 1988	Flora
	AG	5,796,673 365	Aug. 18, 1998	Foss et al.
	AH	6,067,272 365	May 23, 2000	Foss et al.
	AI	6,205,083 365	Mar. 20, 2001	Foss et al.
WK	AJ	5,319,755 395	June 7, 1994	Farmwald et al.
	AK	5,223,755 307	June 29, 1993	Richley
	AA2	5,553,276 395	September 3, 1996	Dean
AK	AB2	5,440,515 365	August 8, 1995	Chang et al.
	AC2			
	AD2			
	AE2			
	AF2			
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	AH2			
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EXAMINER M. TRAA	DATE CONSIDERED 4/2/04
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PTO-1449 REPRODUCED INFORMATION DISCLOSURE CITATION IN AN APPLICATION August 21, 2003 (Use several sheets if necessary)		ATTORNEY DOCKET NO. 2037.1004-007	CONT. OF APPLICATION NO. 10/348,062
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			GROUP

OTHER DOCUMENTS (<i>Including Author, Title, Date, Pertinent Pages, Etc.</i>)		
MT	AR	Nakamura, Kazuyuki, et al., "A 220-MHz Pipelined 16-Mb BiCMOS SRAM with PLL Proportional Self-Timing Generator," <i>IEEE Journal of Solid-State Circuits</i> , Vol. 29, No. 11, pp. 1317-1322(November 1994).
MT	AS	Kushiyama, N., et al., "500 Mbyte/sec Data-Rate 512 Kbits x 9 DRAM Using a Novel I/O Interface," 1992 Symposium on VLSI Circuits Digest of Technical Papers, pp. 66-67 (1992).
MT	AT	Kushiyama, Natsuki, et al., "A 500-Megabyte/s Data-Rate 4.5M DRAM," <i>IEEE Journal of Solid-State Circuits</i> , Vol 28, No. 4, pp. 490-498 (April 1993).
M	AU	Nakamura, Kazuyuki, et al., "A 220MHz Pipelined 16Mb BiCMOS SRAM with PLL Proportional Self-Timing Generator," IEEE International Solid-State Circuits Conference, Session 15, pp. 258-259, 200-201 & 312(February 18, 1994)
	AV	
	AW	
	AX	
	AY	
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	AR2	
	AS2	
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	AU2	
	AV2	
	AW2	

EXAMINER M. TRAN	DATE CONSIDERED 4/1/04
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